11/03/98 JC471 U.S. PTO 09/187197 11/03/98

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PTO/SB/05 (2/98) Approved for use through 09/30/2000 OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MVI-005
First Inventor or Application Identifier	Jacson, Liu
Title	Shallow trench isolation method for a semiconductor wafer.
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [+] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. [+] Specification [Total Pages 16] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [+] Drawing(s) (35 U.S.C. 113) [Total Sheets 7]
4. Oath or Declaration [Total Pages 2]
   a. [+] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference (use only if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [+] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R. §3.73(b) Statement (when there is an assignee) [+] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [ ] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [ ] Other: .....

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17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information below and in a preliminary amendment:
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ____/____
    Prior application information: Examiner _____ Group / Art Unit: _____

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or [+] Correspondence address below

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Name (Print/Type)	Winston Hsu	Registration No. (Attorney/Agent)	41,526
Signature	Winston Hsu	Date	11/3/98

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 830

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Jacson, Liu
Examiner Name	
Group / Art Unit	
Attorney Docket No.	MVI-005

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to

Deposit Account Number

Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 C.F.R. §§ 1.16 and 1.17

☐ Charge the Issue Fee Set in 37 C.F.R. § 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:
☐ Check ☒ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	19 -20** =	0	X	= 0
Independent Claims	2 - 3** =	0	X	= 0
Multiple Dependent				

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,080	228	1,040	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	570	244	285	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Winston Hsu			Reg. Number	41,526
Signature	Winston Hsu	Date	11/3/98	Deposit Account User ID	

Shallow Trench Isolation Method for a Semiconductor Wafer

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a shallow trench isolation method for a semiconductor wafer.

2. Description of the Prior Art

Each MOS transistor component on a semiconductor wafer must be well isolated from neighboring components to prevent interference or short circuiting. In general, localized oxidation isolation (LOCOS) and shallow trench isolation methods are used for isolating the MOS transistors within the semiconductor wafer. Using the LOCOS method a SiO_2 layer (field oxide layer) is formed with an intra-transistor distance of several thousand angstroms by oxidizing the Si substrate of a semiconductor wafer at a high temperature. However, there are always crystal defects associated with generating a field oxide layer with the LOCOS method which include a bird's beak deformity that can affect neighboring components and destroy the integrity of the integrated circuit.

At present, the most commonly used isolation method for isolating MOS transistors in semiconductor processing less than 0.25 μ m is shallow trench isolation. Although this method effectively achieves electrical isolation by filling dielectric material in the shallow trench between any two neighboring components within the semiconductor wafer, there is still a possibility of the "dishing" phenomenon

occurring on the surface of shallow trench. This may affect the electrical performance of the semiconductor wafer. Please refer to Figs.1 to 6. Figs.1 to 6 show the prior art shallow trench isolation method for a semiconductor wafer. As shown in Fig.1, a semiconductor wafer 10 comprises a Si substrate 14, a pad oxide layer 16 formed over the Si substrate 14, and a pad nitride layer 18 deposited above the pad oxide layer 16. The pad oxide layer 16 and pad nitride layer 18 are used as a mask or sacrificial layer during the ion implantation or heat diffusion process which is followed by photolithography and etching to form a plurality of shallow trenches 12 on the surface of the semiconductor wafer 10.

Afterwards, chemical vapor deposition (CVD) is performed to deposit a $Si(OC_2H_5)_4$ (tetra-ethyl-ortho-silicate TEOS) layer and a Poly-Silicon layer in the proper order. As shown in Fig.2, the TEOS layer 20 covers the entire surface of the semiconductor wafer 10 and is used as a dielectric layer, and the Poly-Silicon layer 22 is used as a mask.

At this point, the unnecessary parts of the Poly-Silicon layer 22 are eliminated and the surface of the semiconductor wafer 10 is polished by chemical mechanical polishing (CMP). As shown in Fig.3, the Poly-Silicon 24 in the overlying dishes above the corresponding shallow trenches 12 remain. This makes the surface of the semiconductor wafer 10 flat.

Please refer to Fig. 4. The Poly-Silicon 24 and TEOS layer 20 remaining on the surface of the

semiconductor wafer 10 is etched with reactive ion etching or magnetically enhanced reactive ion etching techniques. The Poly-Silicon 24 remaining after this procedure serves as a mask over the shallow trench 12. After etching, several remaining overhangs 26 are formed above the shallow trenches 12. The remaining TEOS layer 20 and several overhangs 26 are then adjusted to form a tighter structure of solid SiO_2.

CMP is performed to eliminate the remaining overhangs 26 and to polish the surface of the semiconductor wafer 10 making it flat as shown in Fig.5. Finally, the pad oxide layer 16 and pad nitride layer 18 are stripped by etching. As shown in Fig.6, only Si substrate 14 and several shallow trenches 12 of TEOS remain on the surface of semiconductor wafer 10.

When performing CMP and back etching shown in Fig.5 and Fig.6, the overhangs 26 do not work perfectly as masks; therefore, the surface of TEOS in the shallow trench 12 becomes etched. If the shallow trench 12 is big, the surface of TEOS etched is big, and a dish 28 is generated on the surface. The wider the surface, the more severe the dishing which can affect the semiconductor wafer 10. Also, when depositing the film layer, a focusing problem will occur when transferring patterns.

SUMMARY OF THE INVENTION

It is therefore a primary objective of the present invention to provide a shallow trench isolation method of a semiconductor wafer where dishing does not

occur to solve the above mentioned problem.

In a preferred embodiment, the present invention relates to a method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

choosing shallow trenches with widths greater than a predetermined size on the surface of the semiconductor wafer and generating at least one dummy in each chosen shallow trench to form a plurality of new shallow trenches with widths less than the predetermined size;

forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills each shallow trench on the surface of the semiconductor wafer;

condensing the dielectric layer; and

performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each shallow trench with the surface of each component on the semiconductor wafer.

It is an advantage of the present invention that there is no dishing so the semiconductor wafer will not be affected electrically and there will be no focusing problems when transferring patterns.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment which is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 to Fig.6 show the prior art shallow trench isolation method of a semiconductor wafer.

Fig.7 to Fig.11 show a method of forming dummies according to the present invention.

Fig.12 to Fig.14 show another method of forming dummies according to the present invention.

Fig.15 to Fig.16 show a shallow trench isolation method of a semiconductor wafer according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention relates to a shallow trench isolation method of a semiconductor wafer. The method involves first separating large shallow trenches into multiple trenches of smaller width by generating several dummies followed by filling the shallow trenches with dielectric material. Please refer to Fig.7 to Fig.11. Fig.7 to Fig.11 show a method of forming dummies according to the present invention. As shown in Fig.7, a semiconductor wafer 30 comprises a Si substrate 34, a pad oxide layer 36 composed of SiO_2 formed over the Si substrate 34, and a pad nitride layer 38 composed of Si_3N_4 deposited over the pad oxide layer 36. First, shallow isolation trenches are formed on the semiconductor wafer 30. Shallow trenches with widths greater than about 2 μm are used for generating dummies. A plurality of photoresists 32 are applied on the surface of the semiconductor wafer 30 to determine the positions of the shallow trenches by performing photolithography and etching. Then, the surface of the

semiconductor wafer 30 is etched. As shown in Fig.8, the pad oxide layers 36 and pad nitride layers 38 not covered by photoresists 32 are etched to the Si substrate 34.

As shown in Fig.9, photolithography and etching are used to place several photoresists 40 at a uniform distance on the surface of the Si substrate 34. Then, the surface of the Si substrate 34 not covered by photoresists 40 is etched. As shown in Fig.10, several small shallow trenches 42, 44 are formed on the surface of the Si substrate 34. Finally, all photoresists 32 on the surface of the semiconductor wafer 30 are etched. As shown in Fig.11, a small shallow trench 44 and a big shallow trench 46 are formed on the surface of the semiconductor wafer 30, and the shallow trench 46 is separated into several small shallow trenches 42 separated by a uniform distance by several dummies 48. In addition, the preferred height of the dummy is around 300 Å to 500 Å.

Also, because of different degrees of exposure (the areas on the optical mask with different light penetration capability), a plurality of dummies are generated at the bottom of the chosen shallow trenches at the time the shallow trenches are first formed. Please refer to Fig.12. Fig.12 shows the second method of forming dummies according to the present invention. In this scheme, one mask photo is used to place an optical mask 60 above the semiconductor wafer 30 and to expose and transfer patterns by using different light penetration capability on the optical mask 60. The surface of the semiconductor wafer 30 comprises a

Si substrate 34, a pad oxide layer 36, a pad nitride layer 38 and a positive photoresist layer 62. The optical mask 60 comprises a plurality of areas (the space parts) of which the light penetration capability is 100%, a plurality of areas (the parts with oblique lines) of which the light penetration capability is 0 % and a plurality of areas (the parts with horizontal lines) of which the light penetration capability is between 0 % to 100 % ; therefore, the corresponding photoresists 64 are either completely dissolved, not dissolved at all or partly dissolved on the positive photoresist layer 62 of semiconductor wafer 30 and used as masks. Thus, after etching is repeated, the semiconductor wafer 30 with a plurality of dummies and shallow trenches, as shown in Fig.11, is made.

Please refer to Fig.13 and Fig.14. Fig.13 and Fig.14 show the third method of forming dummies according to the present invention and is similar with the second method shown in Fig.12. In the third method, a plurality of photoresists 72 is generated by exposing with different degrees of decomposition on the semiconductor wafer 30 twice. Three groups of photoresists 72, completely dissolved, undissolved and partly dissolved, are formed on the surface of semiconductor wafer 30 and are used as masks when etching. As shown in Fig.13, the method requires being exposed twice. First, a plurality of undissolved photoresists 85 are applied to the surface of semiconductor wafer 30 by using an optical mask 80 with areas with light penetration capability of 100% (the space parts) and areas with light penetration

capability of 0% (the parts with oblique lines). Next, the photoresists 74 that determine the positions of dummies and new shallow trenches are partly dissolved by using another optical mask 90 (as shown Fig.14) comprising both areas with light penetration capability of 100% (the space parts) and 0% (the parts with oblique lines). After etching, the semiconductor wafer 30 with a plurality of dummies and shallow trenches as shown in Fig.11 is made.

Please refer to Figs.15 to 17. Figs.15 to 17 show a shallow trench isolation method of a semiconductor wafer according to the present invention. After the dummies 48 and small shallow trenches are formed, a TEOS layer 50 is deposited over the surface of the semiconductor wafer 30 by performing CVD. The atoms in the TEOS layer 50 are rearranged by annealing to reduce the defect density of the TEOS layer 50 and to tighten the structure of SiO_2. When a plurality of dummies 48 are filled in the big shallow trench 46, the difference between the length of the TEOS layer 50 deposited over the big shallow trench 46 and the length of the TEOS layer 50 deposited over the other parts of the surface of the semiconductor wafer 30 is reduced. Therefore, the TEOS layer 50 deposited over the surface of the semiconductor wafer 30 is a flat surface.

After tightening the TEOS layer 50, the surface of semiconductor wafer 30 is polished by performing CMP. Fig.16 shows polishing of the surface of the pad nitride layers 38 of the semiconductor wafer 30. Finally, the pad oxide layers 36 and pad nitride layers 38 are etched. As shown in Fig.17, only Si substrate 34 and several

shallow trenches 42 comprising TEOS are on the surface of semiconductor wafer 30 which is an intact plane, and the dishing on the surface of TEOS in each shallow trench 42 can be avoided.

Compared with the prior art, the shallow trench isolation method according to the present invention is to first generate several dummies in the bigger shallow trenches to separate the bigger shallow trenches into several shallow trenches with smaller widths to make the surface of the TEOS layer 50 deposited over the surface of the semiconductor wafer 30 flat. At the same time, the TEOS layer 50 is directly annealed without performing reactive ion etching or magnetically enhanced reactive ion etching. The result is an intact plane as the surface of the semiconductor wafer 30. Without dishing, the semiconductor wafer 30 will not be affected electrically and there will be no focusing problems when transferring patterns.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

What is claimed is :

1. A method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

choosing shallow trenches with widths greater than a predetermined size on the surface of the semiconductor wafer and generating at least one dummy in each chosen shallow trench to form a plurality of shallow trenches with widths less than the predetermined size;

forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills each shallow trench on the surface of the semiconductor wafer;

condensing the dielectric layer; and

performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each shallow trench with the surface of each component on the semiconductor wafer.

2. The shallow trench isolation method of claim 1 wherein the predetermined size for the chosen shallow trenches is about 2 μm.

3. The shallow trench isolation method of claim 1 wherein the preferred height of any dummy is around 300 Å to 500 Å.

4. The shallow trench isolation method of claim 1 wherein the planarization process performed on the

dielectric layer surface is a chemical mechanical polishing process.

5. The shallow trench isolation method of claim 1 wherein each component on the semiconductor wafer surface comprises a Si substrate, a pad oxide layer above the Si substrate, and a pad nitride layer above the pad oxide layer, and the planarization process performed on the dielectric layer surface makes this surface inside each shallow trench align approximately with the pad nitride layer of each component on the semiconductor wafer surface; wherein the shallow trench isolation method further comprises:

performing a second planarization process to strip off the pad oxide layer and pad nitride layer from each component, and make the surface of the dielectric layer inside each shallow trench approximately align with the surface of the Si substrate of each component.

6. The shallow trench isolation method of claim 5 wherein the bottom of each shallow trench on the semiconductor wafer is formed by a Si substrate, and each dummy formed in each chosen shallow trench is also made of Si.

7. The shallow trench isolation method of claim 6 wherein after the second planarization process, the dielectric material formed in each chosen shallow trench remains covered over each Si dummy for electrical isolation.

8. The shallow trench isolation method of claim 5 wherein the second planarization process is an etch process.

9. The shallow trench isolation method of claim 5 wherein the pad oxide layer and pad nitride layer are used as a mask or a sacrificial layer during a previous ion implantation or heat diffusion process.

10. The shallow trench isolation method of claim 1 wherein the dielectric layer is condensed by using an annealing process.

11. The shallow trench isolation method of claim 10 wherein the dielectric layer is deposited on the surface of the semiconductor wafer by using a chemical vapor deposition process and the dielectric layer comprises $Si(OC_2H_5)_4$ (tetra-ethyl-ortho-silicate, TEOS) in it.

12. The shallow trench isolation method of claim 1 wherein the dummy within each chosen shallow trench is generated by using a photolithography and etching process, and each dummy is formed at the bottom of each shallow trench.

13. The shallow trench isolation method of claim 1 wherein the dummy within each chosen shallow trench is generated simultaneously when the shallow trench is created.

14. A semiconductor wafer comprising:

a Si substrate;

a plurality of components positioned on the Si substrate, and each pair of neighboring components having a shallow trench between them for isolating the two components;

a dielectric material filled in each shallow trench for electrically isolating the two components on two sides of the shallow trench;

wherein for shallow trenches with widths greater than a predetermined size, at least one dummy is generated at the bottom of each of the shallow trenches to form a plurality of new shallow trenches with widths less than the predetermined size, and the dielectric material filled in each of the shallow trenches covers above each dummy to achieve electrical isolation.

15. The shallow trench isolation method of claim 14 wherein the predetermined size for the chosen shallow trenches is 2 μm.

16. The shallow trench isolation method of claim 14 wherein the preferred height of any dummy is around 300 Å to 500 Å.

17. The semiconductor wafer of claim 14 wherein each dummy is formed of Si, and the method for forming the shallow trenches and the dummies on the semiconductor wafer comprises:

performing a photolithography and etching method on the surface of the semiconductor wafer down to at least the Si substrate to make the shallow

trenches between each component;

applying photoresist to each dummy's position at the bottom of each shallow trench which is wider than the predetermined size;

etching all the shallow trenches on the surface of the semiconductor wafer again to complete all the shallow trenches and the dummies; and

stripping off the photoresists on the semiconductor wafer.

18. The semiconductor wafer of claim 14 wherein the method for forming all the shallow trenches and dummies comprises:

using a photomask to define the positions of all the shallow trenches and dummies on the surface of the semiconductor wafer; and

performing a photolithography and etching method to form the shallow trenches and dummies simultaneously.

19. The semiconductor wafer of claim 18 wherein when performing the photolithography and etching method, the semiconductor wafer is covered with a photoresist layer, and the photomask contains a plurality of transparent areas with different light penetration capability for defining the positions of all the shallow trenches and the dummies on the semiconductor wafer so that the amount of light emitted through the photomask to the photoresist layer over each shallow trench's position is different from the amount of light emitted to each dummy's position whereby all the shallow trenches and the dummies can be formed at

the same time by using the photomask and the photoresist layer.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a shallow trench isolation method of a semiconductor wafer which fills dielectric material into shallow trenches between components on the surface of the semiconductor wafer to electrically isolate the components. This method can prevent dishing phenomenon from occurring over the surface of some wider shallow trenches when a chemical-mechanical polishing method is used to polish the surface of the dielectric material filled in each shallow trench. The method comprises: (1) choosing the shallow trenches with widths greater than a predetermined size and generating at least one dummy in each chosen shallow trench to form a plurality of new trenches with widths less than the predetermined size; (2) covering the surface of the semiconductor wafer with dielectric material to form a dielectric layer; (3) condensing the dielectric layer; (4) polishing the surface of the dielectric layer filled in all the shallow trenches to align the surface of the dielectric material with the surface of the components on the semiconductor wafer.

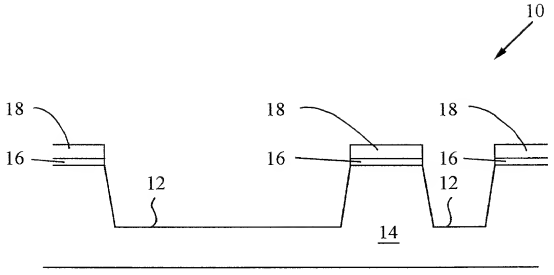

FIG. 1

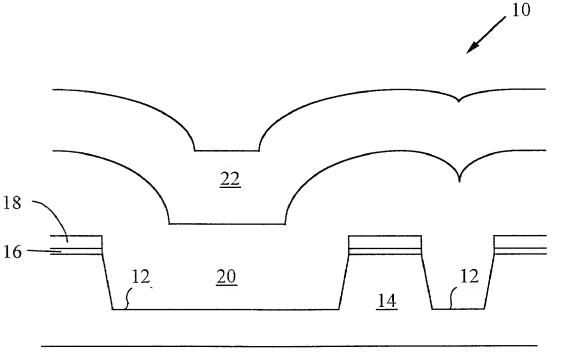

FIG. 2

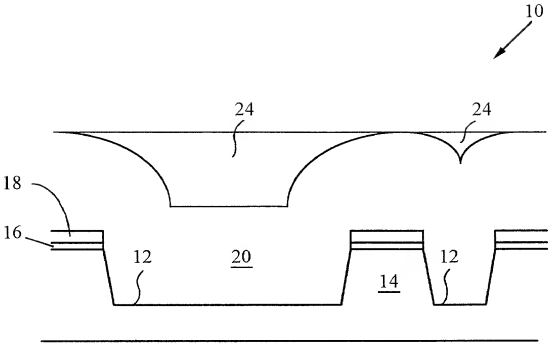

FIG. 3

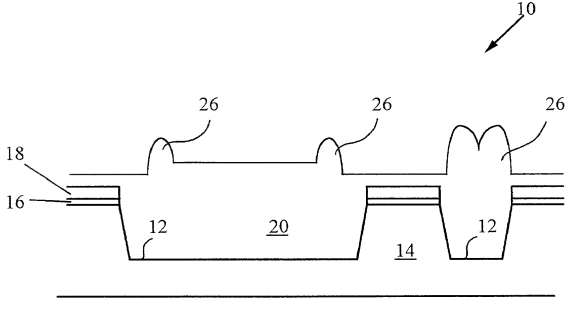

FIG. 4

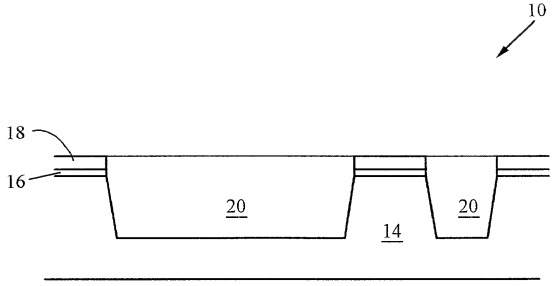

FIG. 5

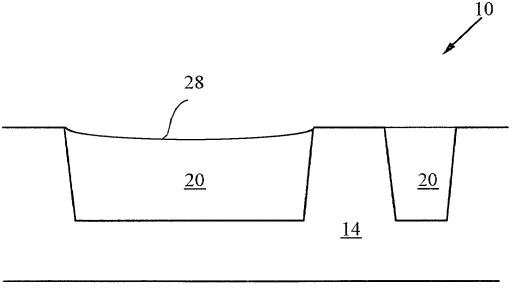

FIG. 6

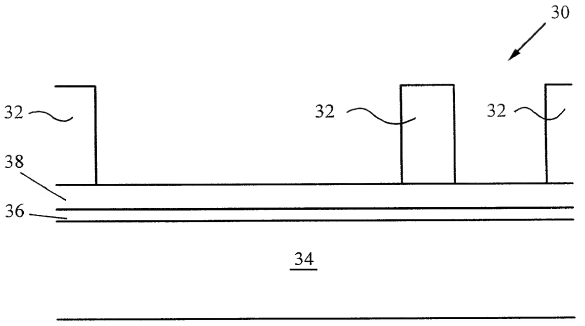

FIG. 7

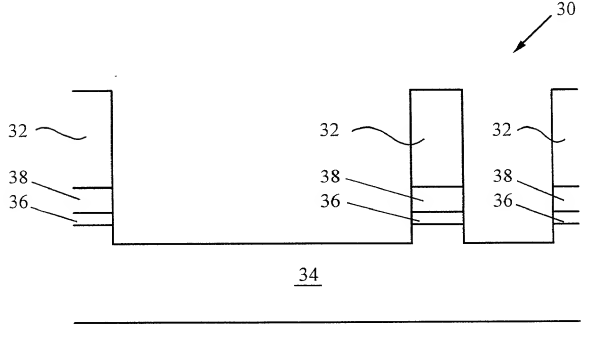

FIG. 8

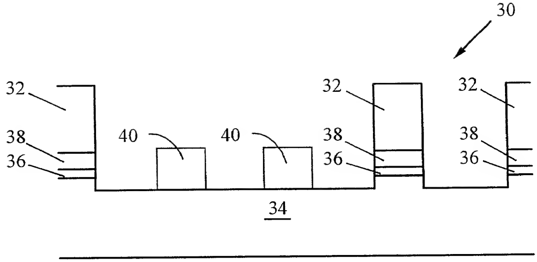

FIG. 9

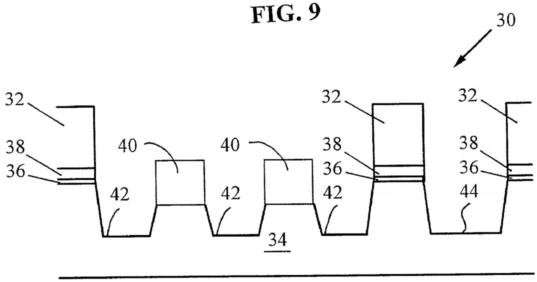

FIG. 10

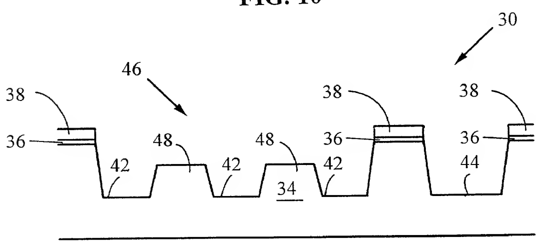

FIG. 11

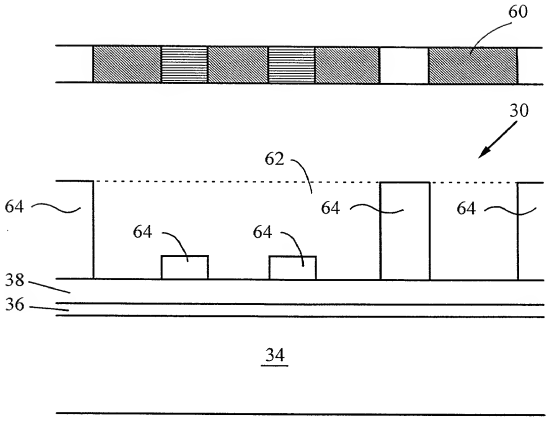

FIG. 12

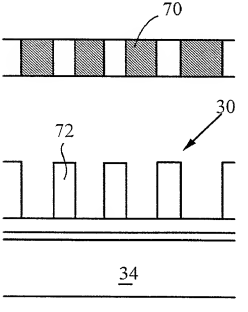

FIG. 13

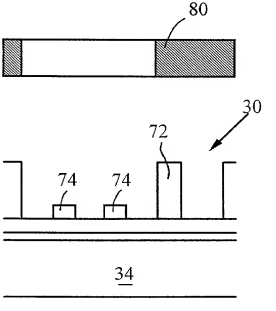

FIG. 14

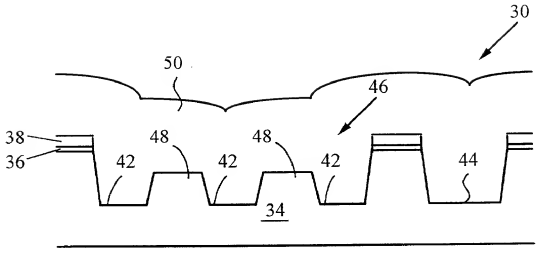

FIG. 15

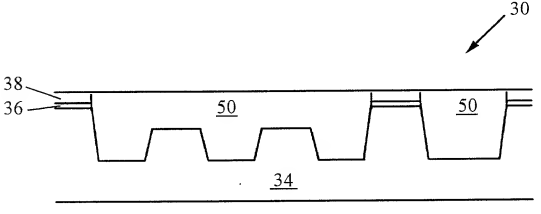

FIG. 16

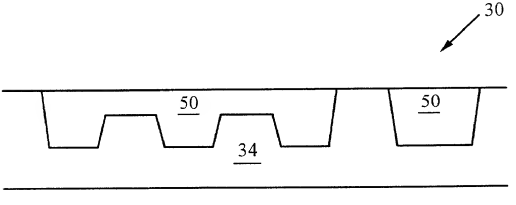

FIG. 17

PATENT
Docket no. MVI - 005

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

I believe I am the sole (if only one name appears below), or a joint (if more than one name appears), original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:
Shallow trench isolation method for a semiconductor wafer.

__+__The specification for the above entitled invention is filed herewith.

_____The specification for the above entitled invention was filed previously with application serial number_____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

__+__There is no claim of priority.

_____Claim of priority is based on the following:

_____

_____

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney to prosecute this application and to transact all related business in the Patent and Trademark Office:

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

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Citizen of: